State of the art of high switching frequency inductive DC-DC converters in SoC context

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Abstract

- Supplying large system on chip requires specific grid and is spread over multiple voltage domains. Each domain depends on a dedicated DC-DC. For the sake of integration, switch capacitor DC-DC seems to have the favors of designers but further increase in the switching frequency associated to a 3D approach gives back some competitiveness to inductive DC-DC converters.
- Some recent experiments in the +100 MHz switching frequency area demonstrate the interest of multiphase and coupled inductors. A global analysis of pertinent results as state of the art enables to draw similar conclusions and many other trends.
- Various landscapes have been populated with available figures in pertinent papers about implemented DC-DC converters. Trends are analyzed to exhibit design trade-offs and further extrapolations, focusing mainly on active devices.
- In the context of POWERSWIPE project, a 200 MHz DC-DC converter (3.3 V input voltage, 350 mW output power, 1.2 V to 0.6 V output voltage) is taken as a study case. Specifications are added in the landscape and the trend analysis orientates the converter architecture for 40 nm CMOS technology. Particularly, cascode-based power stage is analyzed and selected. Primary post-layout simulation results let hope more than 90% power efficiency. Passive devices are related to an interposer technology targeting the fabrication of magnetic devices on top of embedded capacitor banks.

Agenda

- Remember PowerSoC 2012
- Inductive vs. capacitive (non-isolated) DC/DC
- Why +100MHz switching frequency DC/DC ?
- A possible lecture of the state-of-the-art
- PowerSWIPE proposal, early results
- Perspectives

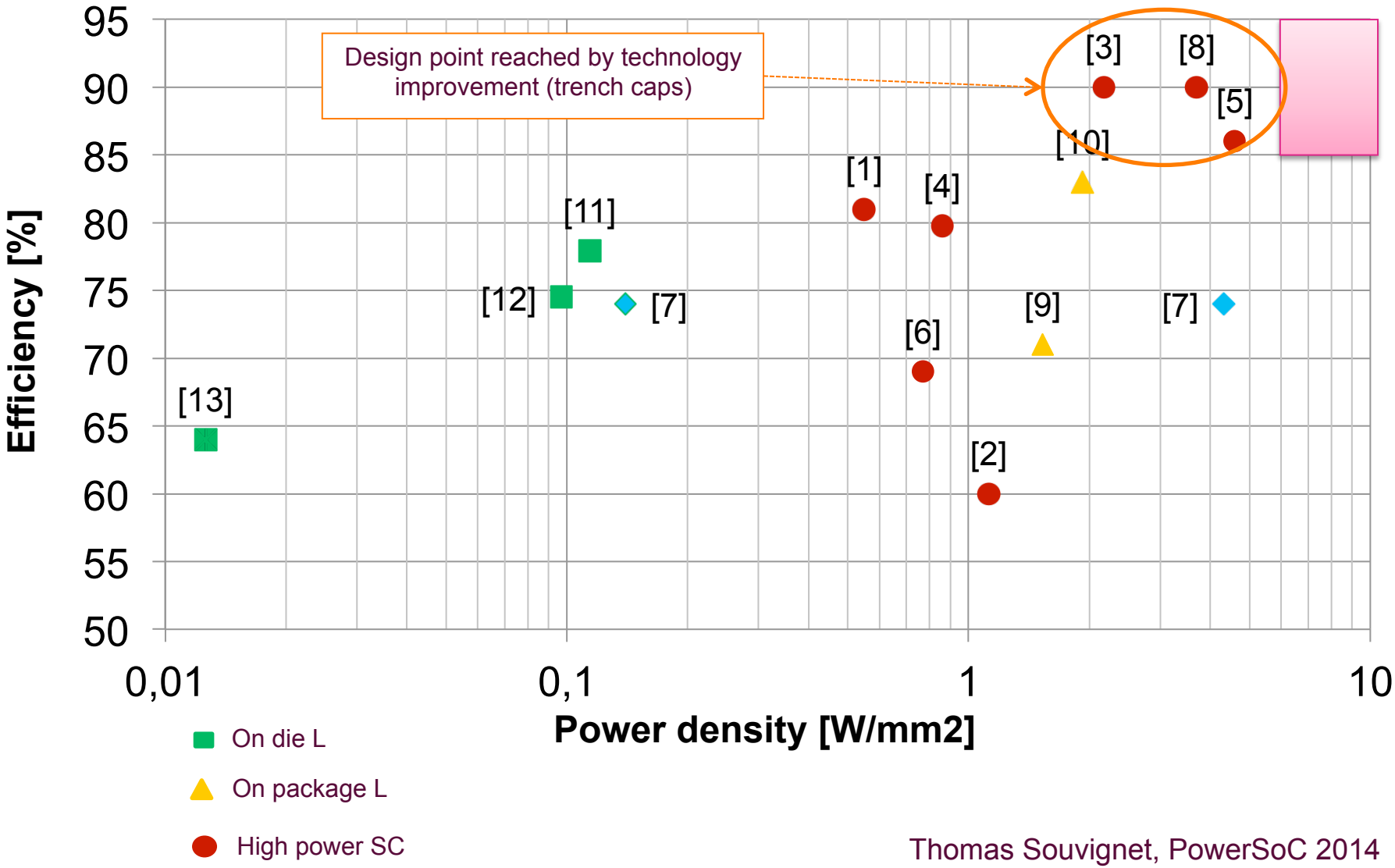
- **Now established: “power is not an afterthought of system”**
- **Specifications now common in essence**
  - how to deliver as much Amps as possible in a given area, for a targeted quality of service, with the best efficiency and the lowest cost
- **Higher expectations: losses < 10% of platform power + efficiency flatness**
- **Global view: passives as important as actives**
- **Complex control schemes despite high switching frequency**

Non-isolated DC/DC converters

Inductive versus capacitive architectures

- SoA → efforts to push the limits
- SoC → heavy technology constraint
- V_{out}/V_{in} specification
- Necessity for a portfolio of solutions with various trade-offs

Capacitive on-chip DC/DC



Thomas Souvignet, PowerSoC 2014

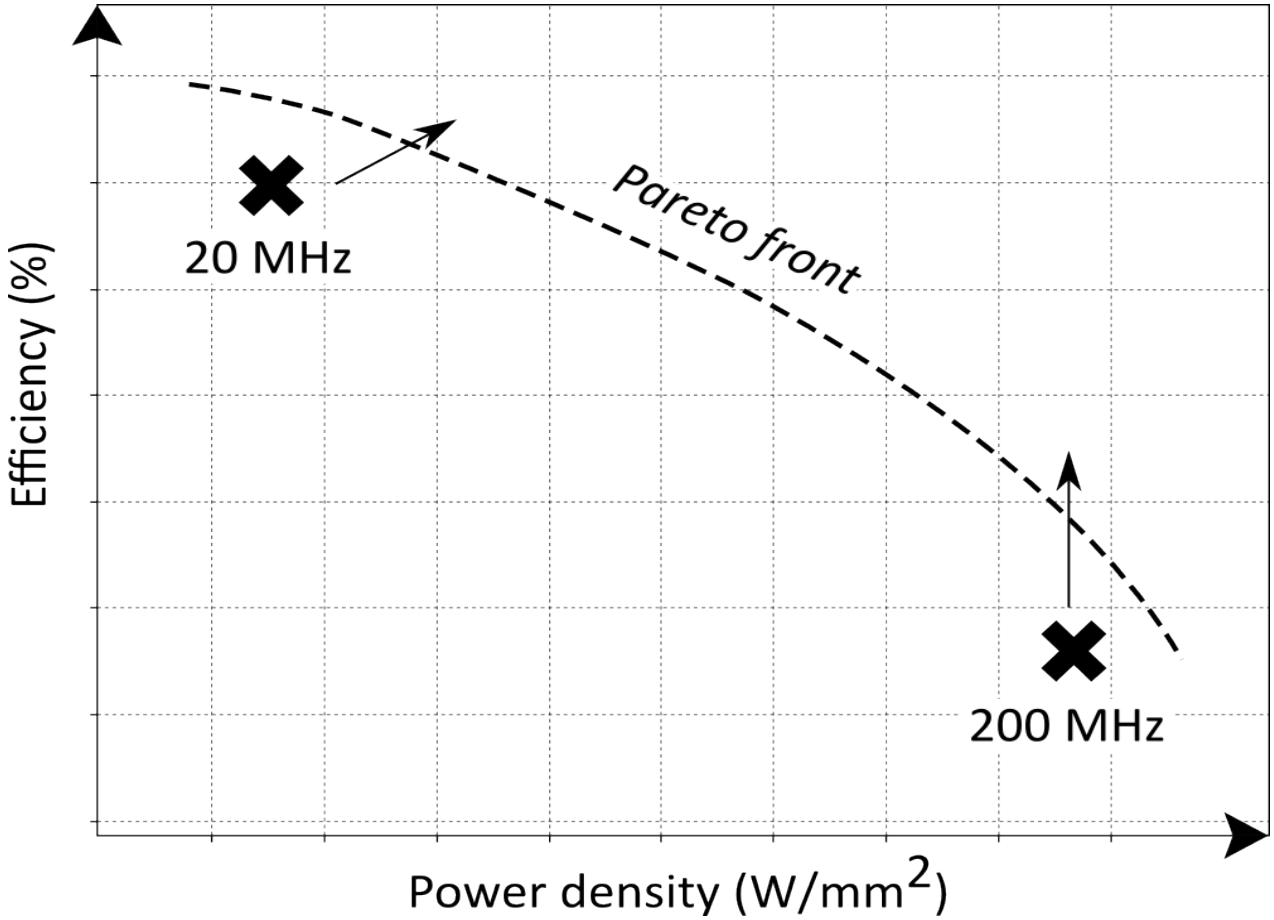
Non-isolated DC/DC converters

Why +100MHz switching frequency ?

- Improvements in technology enables better active and passive devices → mechanical increase in frequency thus in footprint
- Application requirements
  - large transient performances (EER, DVFS)
  - power density (smaller footprint)
- Mission profile (efficiency flatness)

Why +100MHz switching frequency ?

↳Losses → limit voltage and frequency, but…



J.W. Kolar et al., “PWM Converter Power Density Barriers”, IEEE PCC, 2007

State-of-the-art of HF DC-DC

Silicon demonstrators

- Steady-state performances
- Transient performances, Power density aspects: no common benchmarks

Many metrics, unique FoM not pertinent → landscapes

Reference point :

[Burton et al., 2014] Fully integrated voltage regulators on 4th generation Intel core SoCs. In 29th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2014, pages 432-439.

CIPS 2014: Neveu, F.; Martin, C.; Allard, B., "Review of high frequency, highly integrated inductive DC-DC converters", 8th International Conference on Integrated Power Systems (CIPS), 2014, pp.1-7, 25-27 Feb. 2014

State of the art - References

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[Li, 2012] A fully-integrated buck converter design and implementation for on-chip power supplies. Journal of Computers, 7(5):1270–1277.

[Lu et al., 2012] A 1500ma, 10mhz on-time controlled buck converter with ripple compensation and efficiency optimization. In Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, pages 1232 –1237.

[Maity et al., 2011] Design of a 20 mhz dc-dc buck converter with 84 percent efficiency for portable applications. In VLSI Design, 2011 24th International Conference on, pages 316–321.

[Onizuka et al., 2006] Stacked-chip implementation of on-chip buck converter for power- aware distributed power supply systems. In Solid-State Circuits Conference, 2006. ASSCC 2006. IEEE Asian, pages 127 –130.

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[Peng et al., 2013] A 100 mhz two-phase four-segment dc-dc converter with light load efficiency enhancement in 0.18 µm cmos. Circuits and Systems I: Regular Papers, IEEE Transactions on, 60(8):2213–2224.

[Peng et al., 2011] High efficiency, high switching speed, algaas/gaas p-hemt dc-dc converter for integrated power amplifier modules. Analog Integrated Circuits and Signal Processing, 66:331-348.

[Schrom et al., 2004] A 480-mhz, multi-phase interleaved buck dc-dc converter with hysteretic control. In Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, volume 6, pages 4702–4707 Vol.6.

[Schrom et al., 2007] A 100mhz eight-phase buck converter delivering 12a in 25mm2 using air-core inductors. In Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE, pages 727 –730.

[Song et al., 2014a] A vhf-level fully integrated multi-phase switching converter using bond-wire inductors and on-chip decoupling capacitors and dll phase synchronization. In Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE.

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[Sturcken et al., 2013] A 2.5d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer. Solid-State Circuits, IEEE Journal of, 48(1):244–254.

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[Villar and Alarcon, 2008] Monolithic integration of a 3-level dcm-operated low-floating-capacitor buck converter for dc-dc step-down conversion in standard cmos. In Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, pages 4229 –4235.

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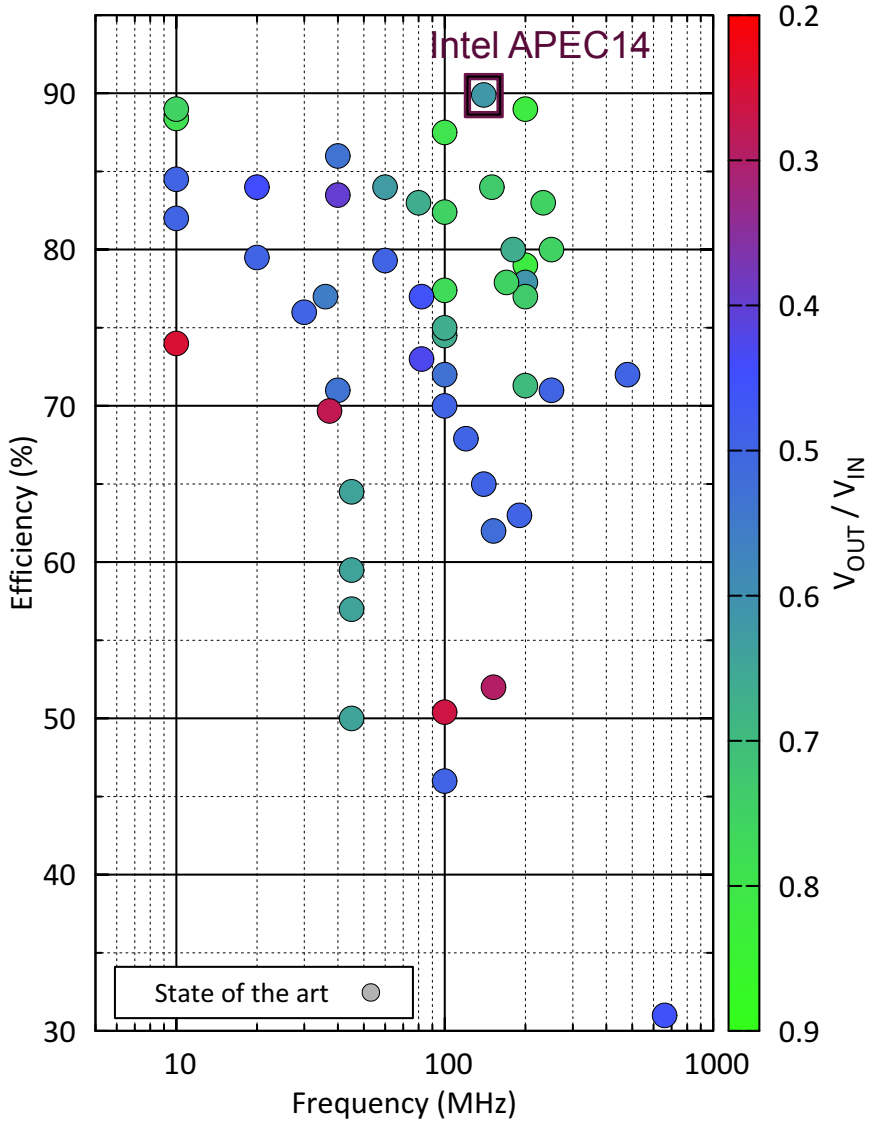
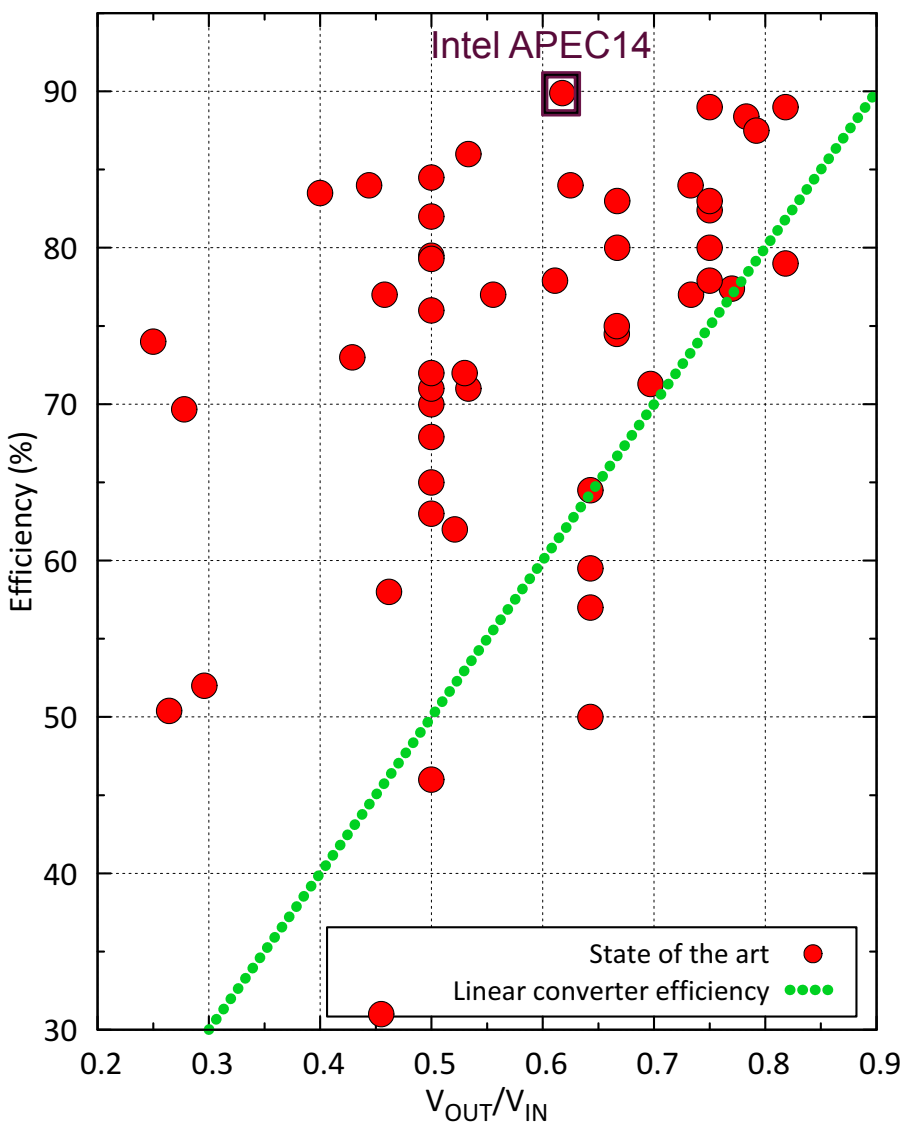
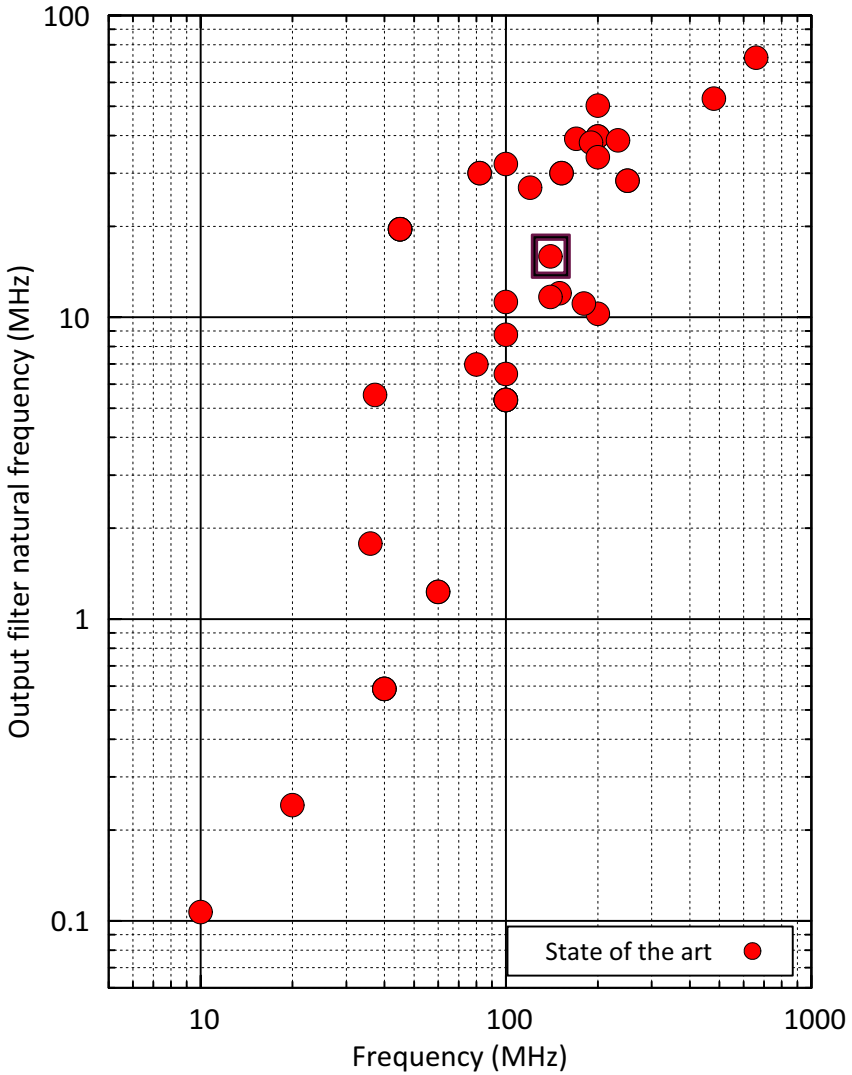
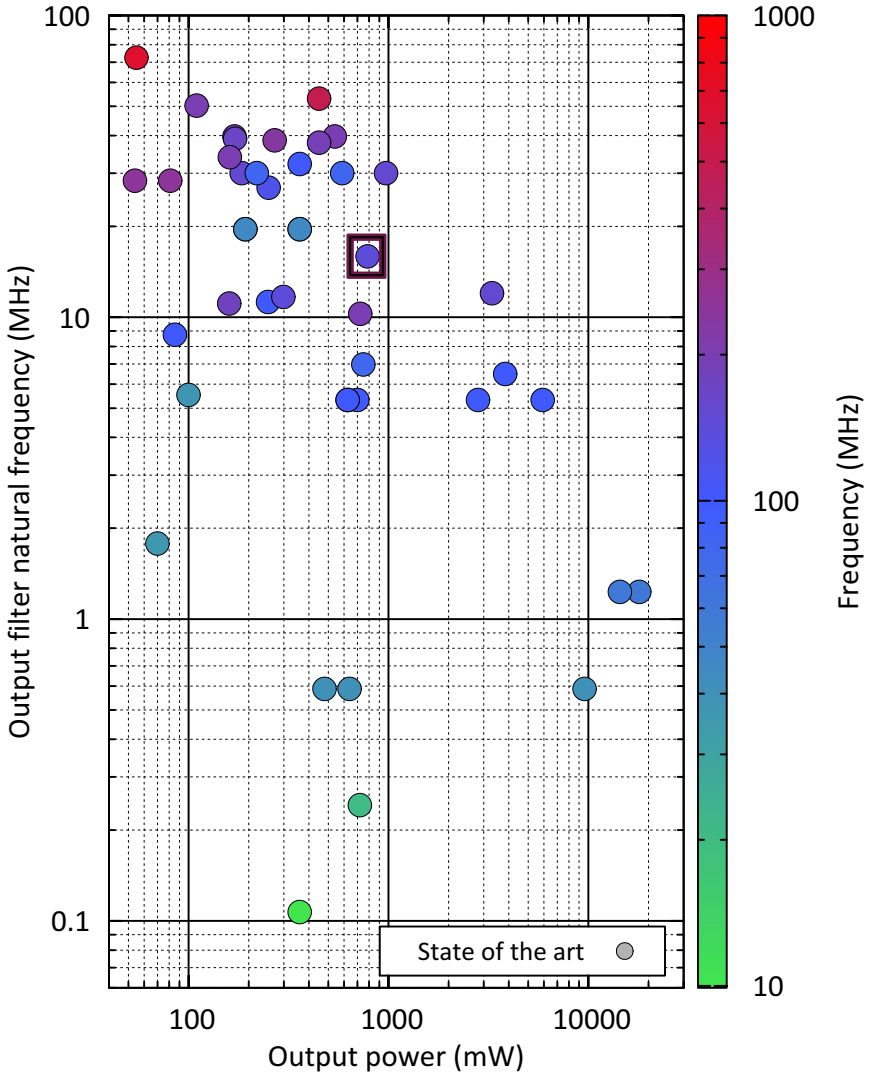
Efficiency, frequency and ratio



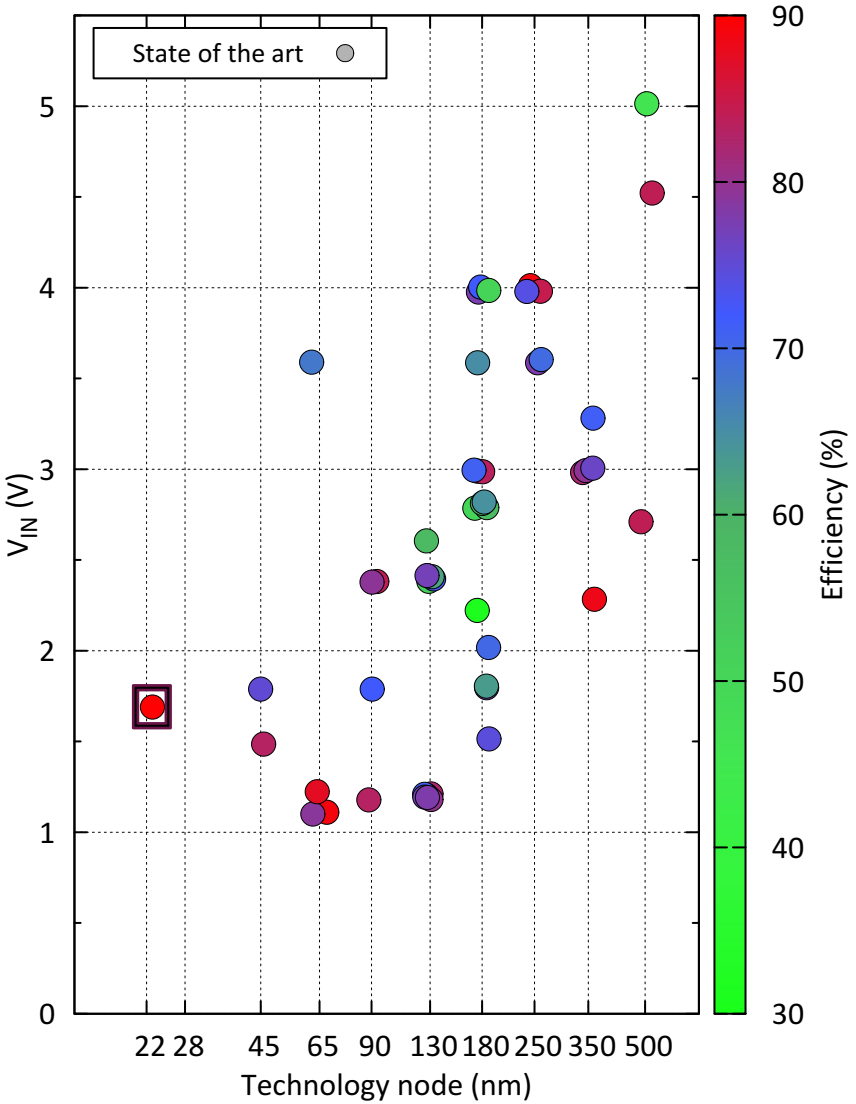


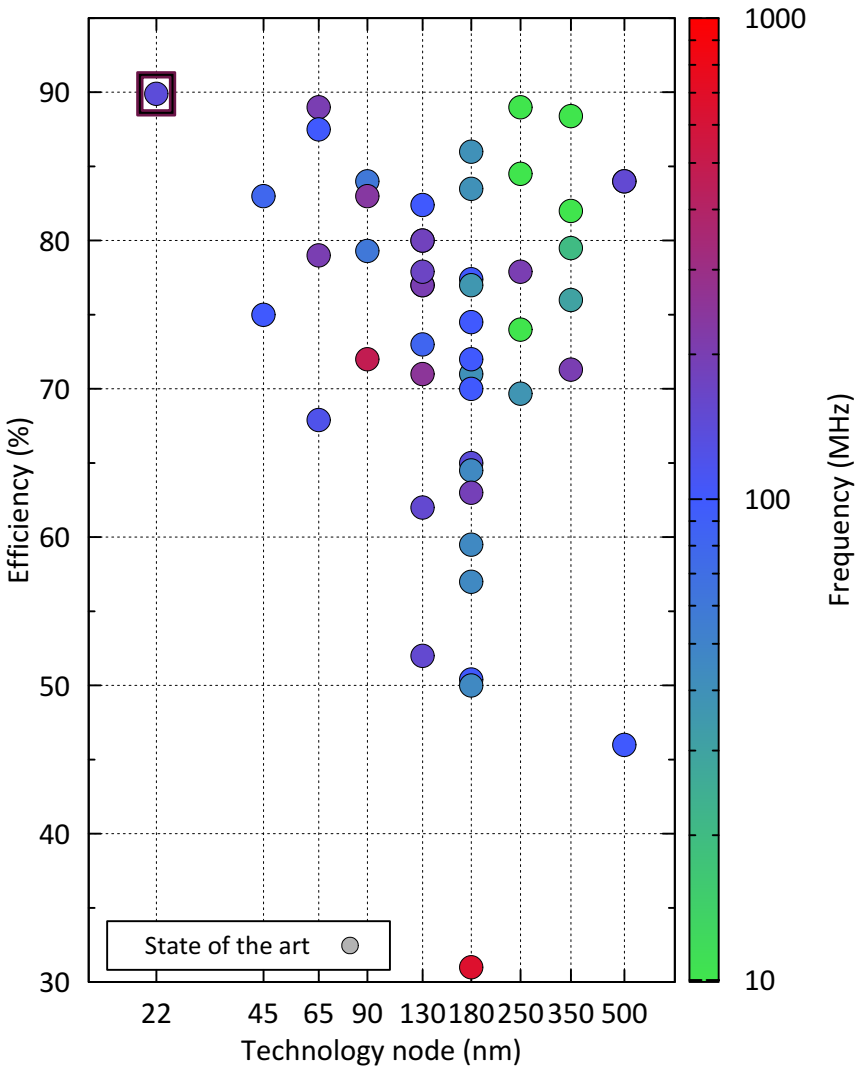
Output filter





Technology


State of the art
V_{IN} (V)
Technology node (nm)
Efficiency (%)
0
1
2
3
4
5
22 28
45
65
90
130
180
250
350
500
30
40
50
60
70
80
90


State of the art
Efficiency (%)
Technology node (nm)
Frequency (MHz)
30
40
50
60
70
80
90
22
45
65
90
130
180
250
350
500
10
100
1000

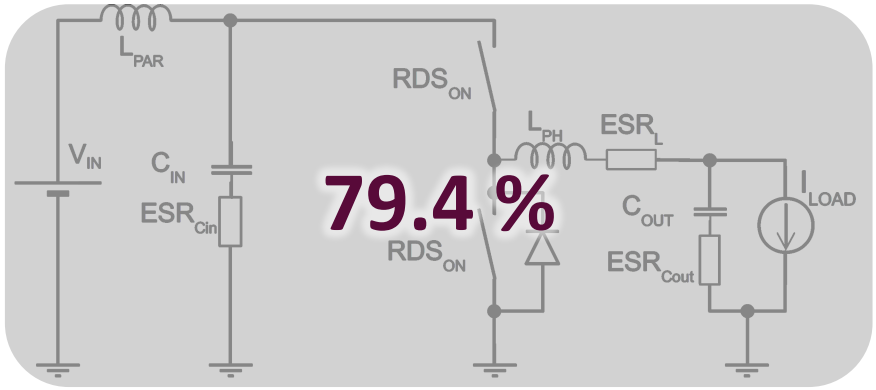
Control schemes

- **Voltage mode versus current mode**
- **PWM versus Hysteretic control or sliding mode control**
- **Digital versus analogue**
  - 2 control loops (analogue control + digital supervisor)
  - Full digital low-losses controller demonstrated (limitations in transient performances)

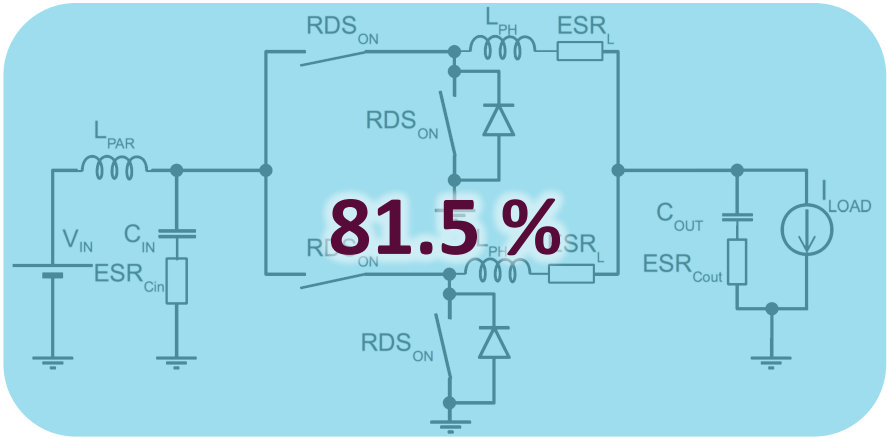
- **Systematic stability of closed-loop DC/DC quite complex (sample data modeling)**
- **CAE quite complex**

Wrap-up

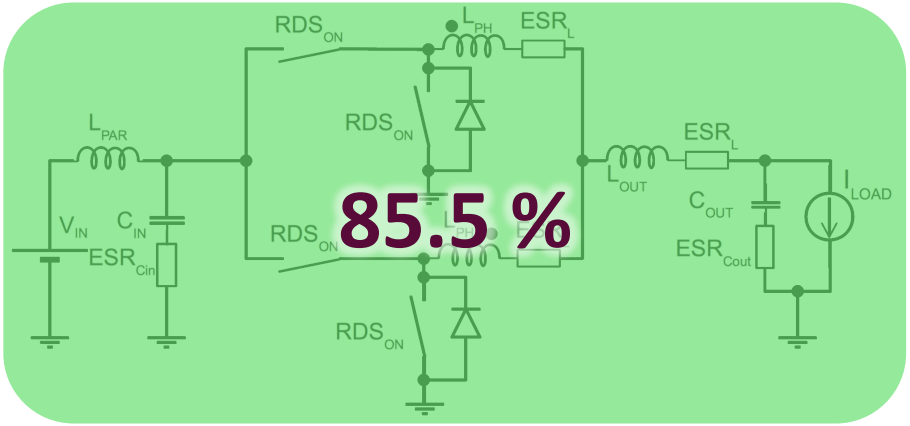
- **+100MHz switching frequency → phase coupling**



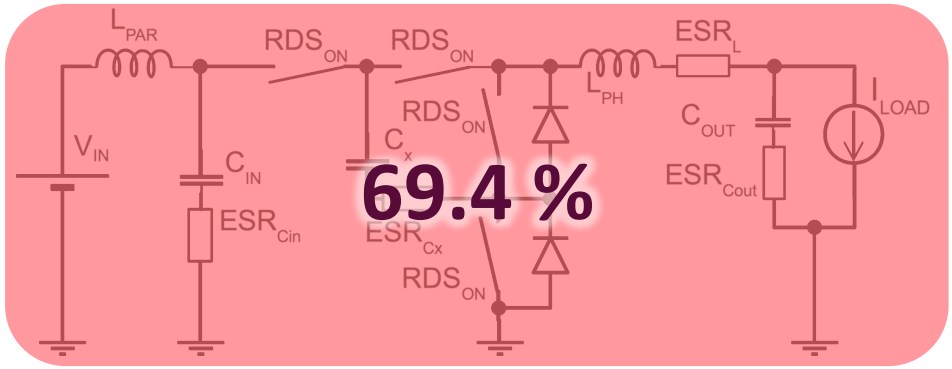
Standard cell



2-phases



Coupled 2-phases



3-levels

Wrap-up

- **Efficiency flatness → phase shedding**

- **Air inductors versus magnetic devices:**
  - Cost, complexity
  - EMI is an issue
  - Coupling of inductors → magnetic material

- **Separate issues, separate technologies**
  - Interposer of passive devices
  - Enable trench capacitors

- **Motivations for PowerSWIPE HF DC/DC**

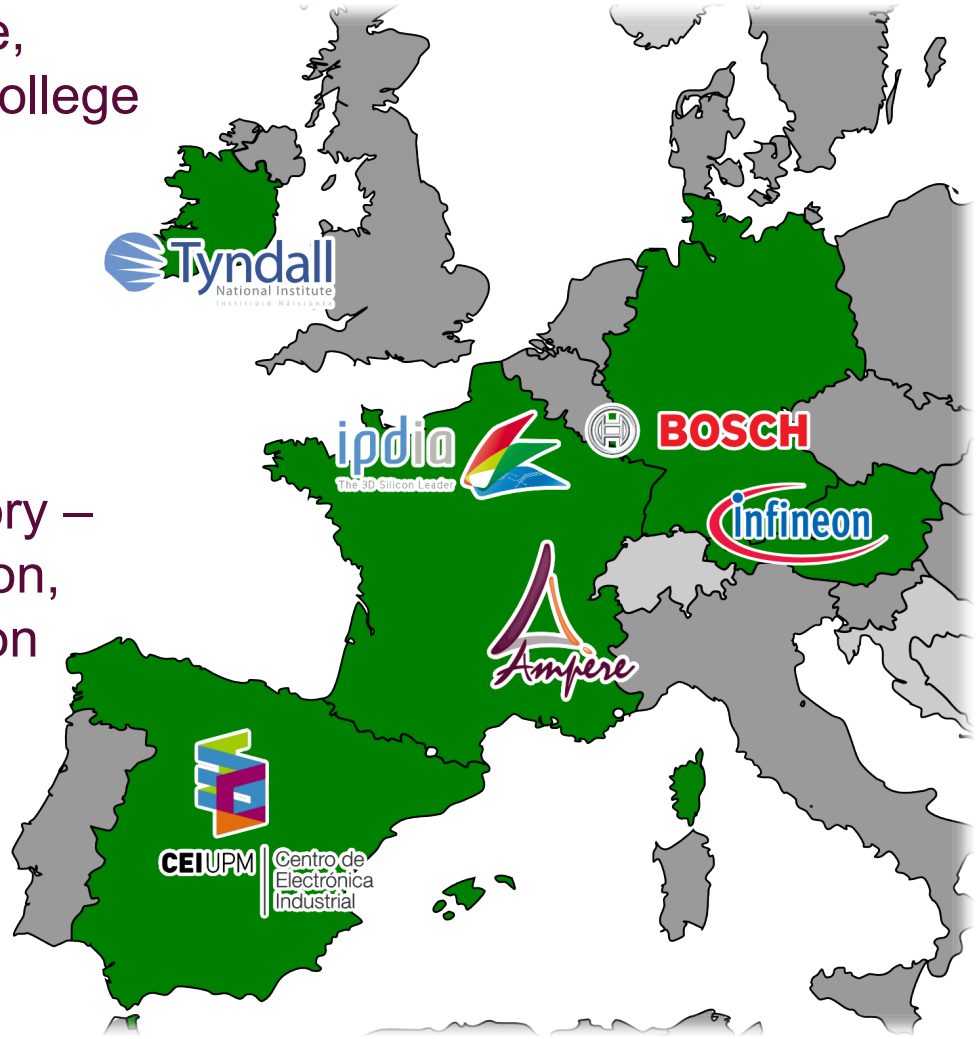
PowerSWIPE consortium

Tyndall National Institute, University College Cork

IPDiA, Caen

Ampère Laboratory – University of Lyon, INSA Lyon, Lyon

Centro de Electrónica Industrial – Universidad Politécnica de Madrid



Robert Bosch GmbH

Infineon Technologies AG

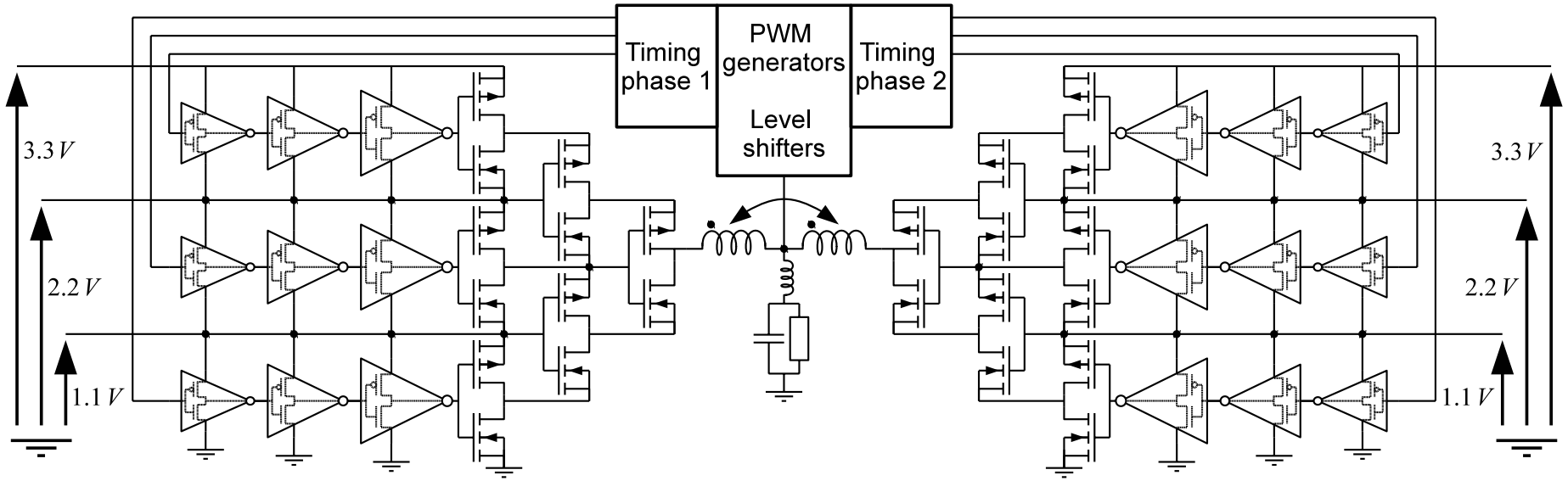
Infineon Technologies Austria Villach AG

Schematic

Kursun, V., Narendra, S. G., De, V. K., & Friedman, E. G. (2005). Cascode monolithic DC-DC converter for reliable operation at high input voltages. Analog Integrated Circuits and Signal Processing, 42(3), 231-238 → **evaluation by simulation**

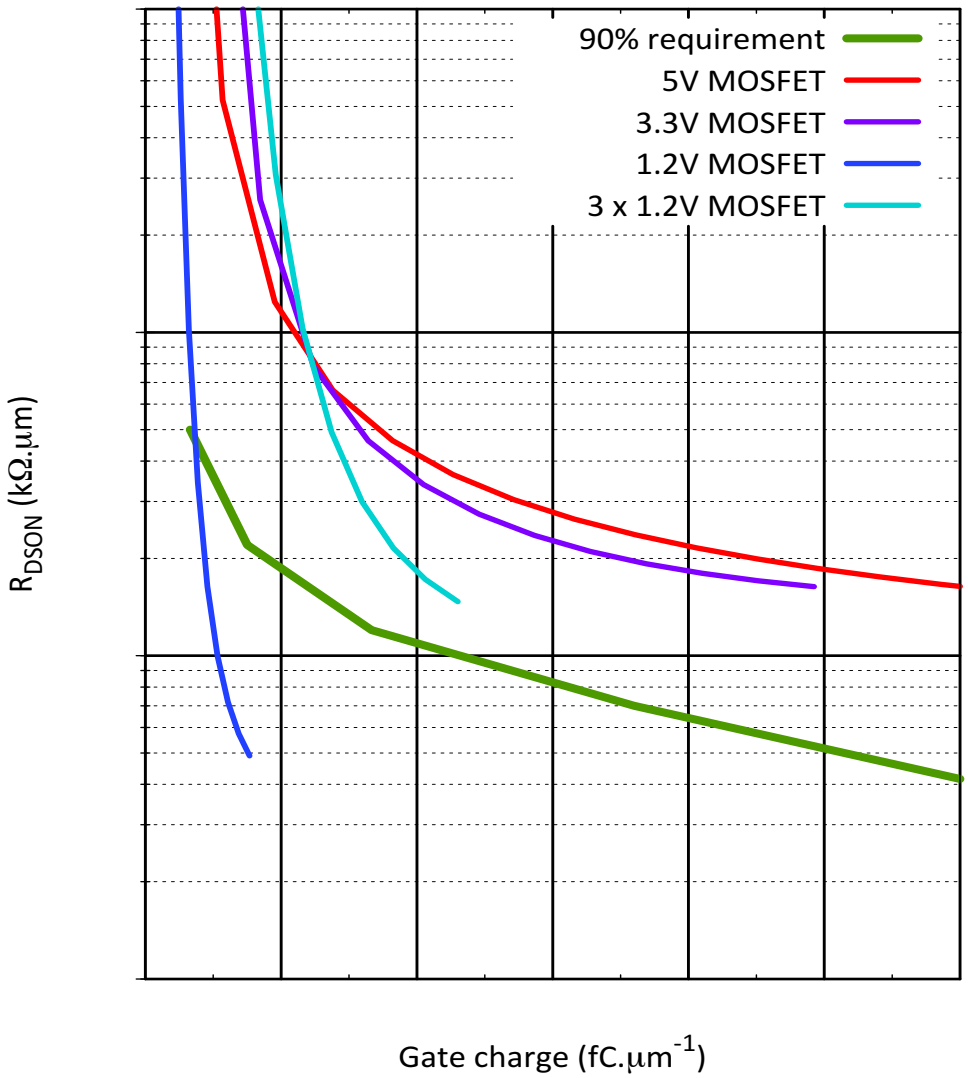
Peng et al., 2013, A 100 MHz two-phase four-segment DC-DC converter with light load efficiency enhancement in 0.18 µm CMOS. IEEE Trans. Circ. & Syst. I, 60(8):2213–2224.

- **40nm bulk CMOS**
- **Interposer by IPDIA and Tyndall**
- **Hard switching then Hysteretic control**



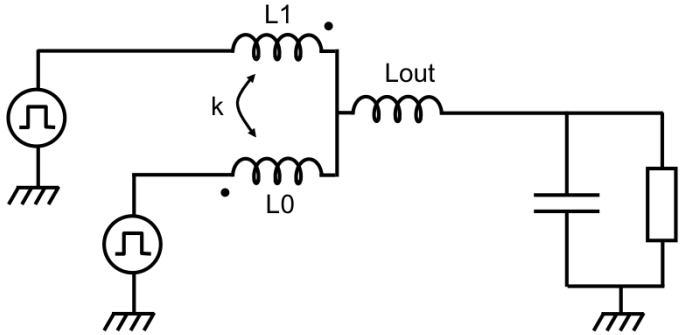
See details on design on poster #9 by Florian Neveu

Motivation for low-voltage MOSFET



- Standard DC/DC step-down
- Analytical model of losses
- Low-voltage MOSFET
- Digital MOSFET could be considered
- Similar conclusions in any thin technology

Local optimization of coupled inductors



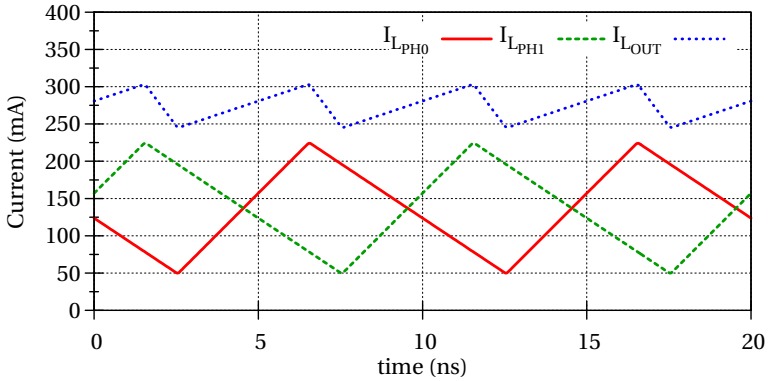
L0 = L1

-1 < k < 1

0 ≤ Lout ≤ 91 nH

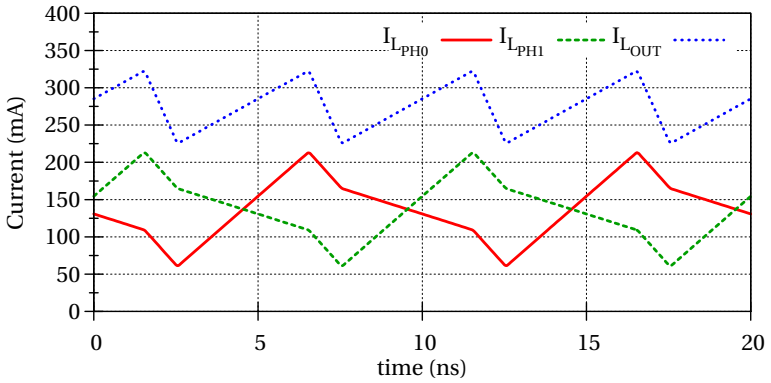
L0 + L1 + Lout = 91 nH

Minimizing phase current ripple



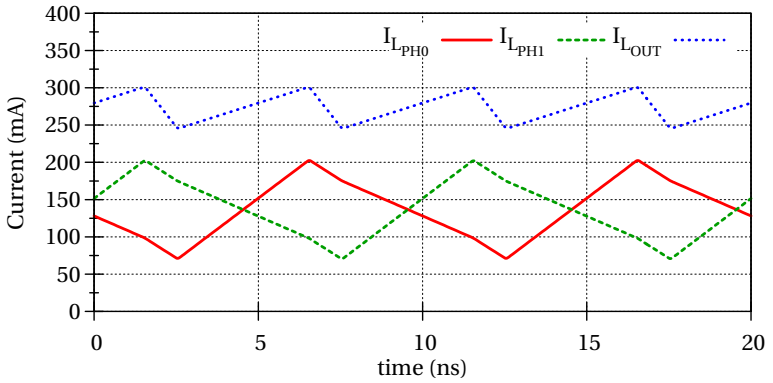
#1: k = 0, L0 = L1 = 45.5 nH, Lout = 0 nH

Ripple: Phases: 172 mA, Output: 56 mA



#2 : Lout = 0 nH, L0 = L1 = 45.5 nH, k = 0.4

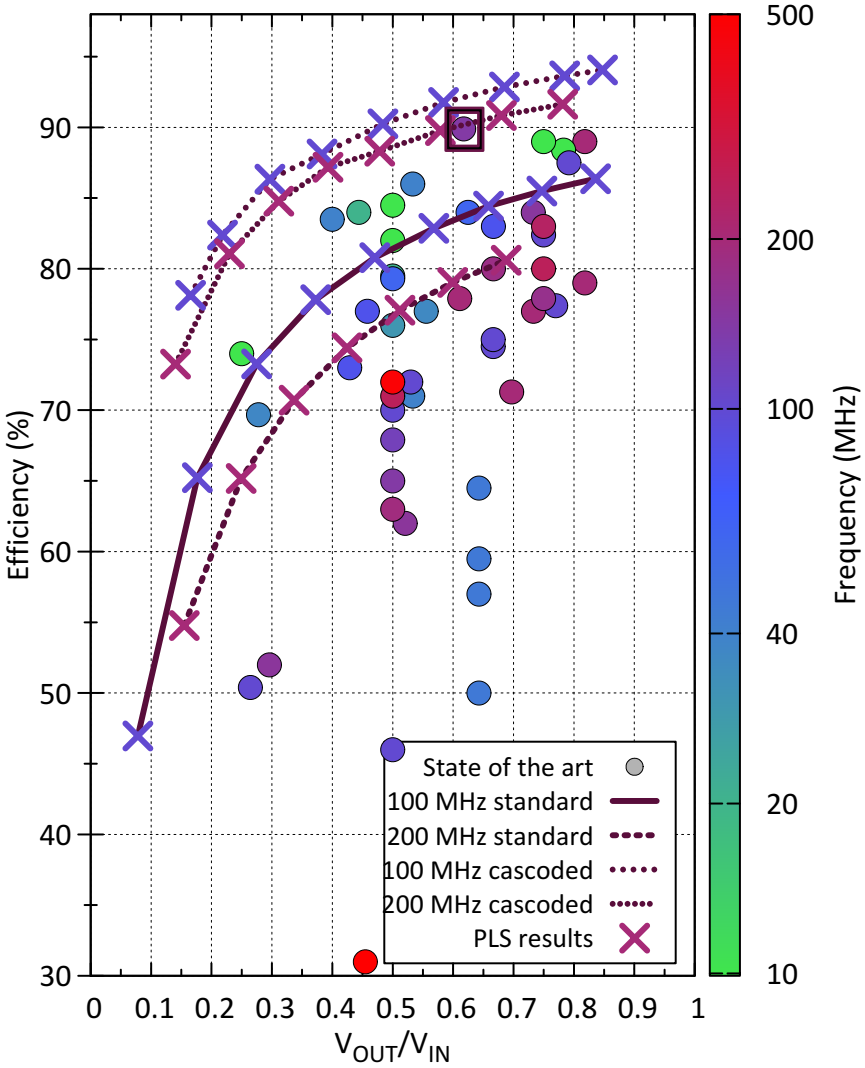
Ripple: Phases: 151 mA, Output: 102 mA

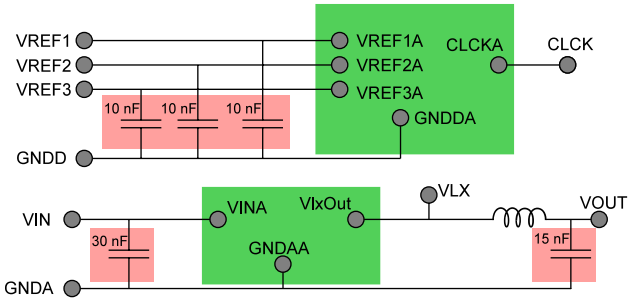


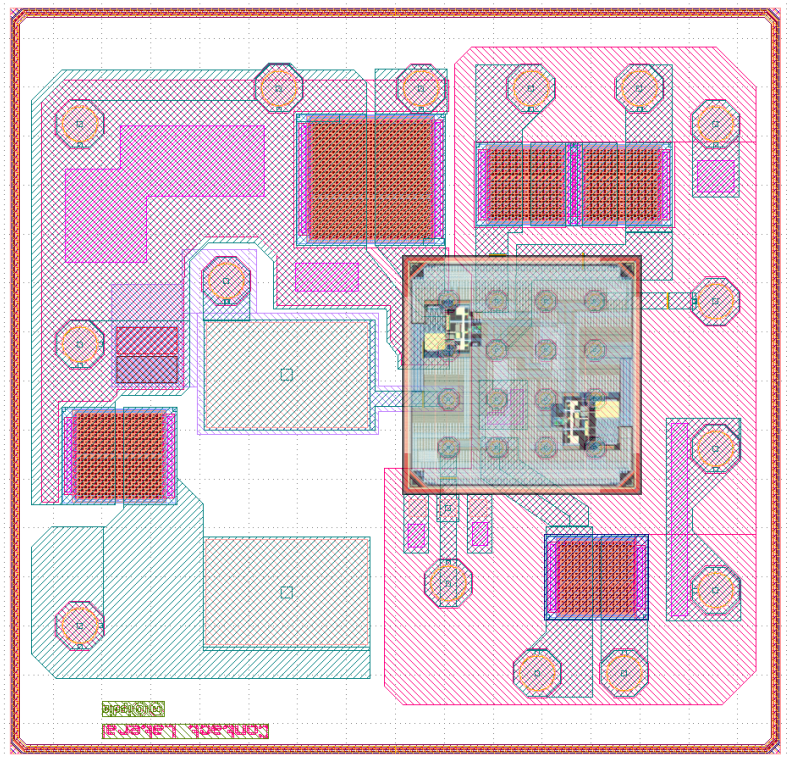
#3: L0 = L1 = 35 nH, Lout = 21 nH, k = 1

Ripple: Phases: 123 mA, Output: 55 mA

Primary PLS results







Perspectives

- Waiting for silicon delivery
- Multi-chip test board
- Verification of limits of robustness

- Multi-phase design
- Optimized IC layout
- Optimized interposer layout